each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches; and

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches;

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches.

(NEW) 30. The device of claim 29, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 31. The device of claim 30, wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

(NEW) 32. The device of claim 29, wherein all of said active trenches are parallel elongated trenches.

(NEW) 33. The device of claim 32, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 34. The device of claim 29, wherein:

at least a plurality of said active trenches containing MOS gated structures are polygonal in topology and are symmetrically spaced and disposed over the surface of said silicon wafer;

said source regions surrounding respective ones of said active trenches containing a MOS gated structure;

said intermediate trenches surrounding said at least a plurality of said active trenches consisting of a trench of lattice shape in topology which extends in the space defined between spaced active trenches having said polygonal to pology.

(NEW) 35. The device of claim 34, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 36. The device of claim 29, wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

(NEW) 37. The device of claim 36, in which said gate dielectric and said bottom dielectric are silicon dioxide.

(NEW) 38. The device of claim 37, wherein said gate dielectric has a thickness which is less than 900 Å.

(NEW) 39. The device of claim 38, wherein the thickness of said bottom dielectric is greater than about 1300 Å.

(NEW) 40. The device of claim 37, wherein the thickness of said bottom dielectric is greater than about 1300 Å.

(NEW) 41. The device of claim 36, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches

and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(NEW) 42. The device of claim 10, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(NEW) 43. The device of claim 42, wherein said concentric rings have a predetermined spacing from one another.

(NEW) 44. The device of claim 43, wherein the spacing between said rings is selected such that breakdown caused by high reverse voltage occurs between said rings before breakdown occurs in said active area.